REMARKS

Claims 1-12 are pending in this application. By this Amendment, claims 1-2, 4-5, 9-10 and 11-12 are amended. No new matter is added. Reconsideration of this application is respectfully requested.

Applicants appreciate the courtesies shown to Applicants' representatives by Examiner Sircus and Examiner Kitov in the June 28 personal interview. During the interview, discussion focused upon the Izawa/Nasila combination. Specifically, Applicants' representatives presented arguments that the proposed modification to Nasila as suggested by the March 11, 2005 Office Action is improper because such a proposed modification is counter to the teachings of Nasila. Additional details regarding the Applicant's position with respect to the Nasila/Izawa combination are provided below.

Applicant submit that entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration; (c) do not present any additional features without canceling a corresponding number of features from dependent claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

Applicants respectfully assert that: 1) even if combined, the Nasila/Izawa combination would not include all features recited in the claims of the present application; 2) the proposed Nasila/Izawa combination is improper because the suggested modifications to Nasila would destroy the intended purpose of the protection circuit described in Nasila, or alternatively, would change the purpose of operation of Nasila; 3) the Nasila and Izawa patents address

issues unrelated to the present application; and, 4) the Nasila/Izawa combination is based upon impermissible hindsight.

For at least these reasons, Applicants respectfully assert that it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution to produce a circuit as described in the present application. Given that the Nasila/Izawa combination is improper, Applicant's respectfully submit that the combination of the Nasila/Izawa combination with any other reference would also be improper.

Further, Applicants would like to emphasize that by adding a feature to an independent claim from a dependent claim, the resulting independent claim is broader than the original dependent claim. Therefore, the scope of the respective independent claims will necessarily have been addressed by the prior art searches already performed by the Examiner. Therefore, the claim amendments do not necessitate further search and/or consideration.

For at least the reasons addressed above, and for at least the reasons detailed below, Applicants respectfully submit that the Amendment is proper and should be entered into the record.

I. 35 U.S.C. §102(b) Rejection of Claims 1 and 4

The Office Action rejects claims 1 and 4 under 35 U.S.C. §102(b) as unpatentable over U.S. Patent No. 6,005,761 to Izawa et al. ("Izawa"). This rejection is respectfully traversed.

Independent claim 1 recites, *inter alia*, "a first resistor interposed between the gate and a source of the FET." Independent claim 4 recites, *inter alia*, "a first resistor interposed on a second connection line between the gate and a source of the FET." These features were previously included in dependent claims 2 and 5, respectively.

Applicants respectfully submit that Izawa does not disclose, teach or suggest the combination of features recited by the respective claims. Accordingly, it is respectfully

submitted that claims 1 and 4 are patentably distinguishable over the applied art. Accordingly, withdrawal of this rejection is respectfully requested.

II. 35 U.S.C. §103(a) Rejection of Claims 1-2, 4, 9, and 11

The Office Action rejects claims 1-2, 4, 9, and 11 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,886,563 to Nasila et al. ("Nasila") in view of Izawa. This rejection is respectfully traversed.

The Office Action states at page 7, lines 5-12, that "both references have the same problem solving area, namely providing power MOS load drivers. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution by removing the second (bottom) transistor together with the Zener diode from the circuit, since as well known in the art, the half-bridge drivers are used only for bipolar driving of the load, and if bipolar driving is not required, as Izawa et al. demonstrated, only one transistor and no Zener diode is necessary. The Izawa circuit has definite advantage in cost of the parts." Applicants respectfully disagree for at least the following reasons.

A. Even if Combined, Nasila and Izawa Would Not Include All Claimed Features

First, even if the circuit in Nasila were modified as described in the Office Action, the resulting circuit would not include all of the features recited in claim 1. For example, if the exemplary circuit in Nasila shown in Figs. 2, 3, 6 or 7 were modified, the resulting circuit would still not include "a first resistor interposed between the gate and a source of the FET," as recited in claim 1. Alternatively, if the exemplary circuit in Nasila shown in Fig. 8 were modified, the resulting circuit would not include "a first connection changer interposed on a connection line between a gate of the FET and a gate drive voltage supply source, the first connection changer changing a connection state between a first connection state in which the

gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground," as recited in claim 1.

B. The Nasila/Izawa Combination is Improper

Second, Applicants respectfully assert that the Nasila/Izawa combination is improper at least because in accordance with MPEP §2143.01, "if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

As stated in Nasila at col. 1, lines 52-61, through col. 2, line 5 with reference to Fig. 1:

> The Achilles' heel of any half-bridge topology is the threat of simultaneous conduction of both ((output)) transistors. If this condition were to occur, damaging currents would flow through Q1 and Q2. Therefore, the designer must guard against this condition by providing a `deadtime` interval, during which both transistors are guaranteed to be OFF. Implementing this deadtime (a measure of the designer's conservatism) increases both the complexity, and the minimum cycle time of the circuit. This explains the need for the `TURN-ON DELAY` block.
>
> It is an object of the invention to provide high speed electronic commutation for power conversion, where a break-before-make sequence of switching of output transistors is assured.
>
> In the circuit to be described, the transistors comprising the half-bridge are electronically interlocked--precluding cross-conduction; and high-side voltage generation and logic level translation are integral to the interlock mechanism. This circuit is simple, robust, and as fast as physics permits.

Based upon the above-cited text, the intended purpose of the circuit described in Nasila is to protect against damaging a circuit with a half-bridge topology due to the simultaneous conduction of both (output) transistors in the circuit. Nasila addresses this problem with a circuit in which "the transistors comprising the half-bridge are electronically interlocked-precluding cross-conduction; and high-side voltage generation and logic level translation are integral to the interlock mechanism." (See col. 2 lines 1-5).

At col. 2, lines 9-17, Nasila states that, "illustrated in FIG. 2 is an ideal Interlocked Half-Bridge schematic. Q1, and Q2 combine to form a half-bridge phase leg. Diode CR2 provides reverse isolation from the GATE to SOURCE of Q1, while permitting forward current through Q2. Observe that if Q2 is conducting, Q1 will be biased OFF through CR2; and that if Q2 is OFF, Q1 will be permitted to conduct, provided it is biased ON. Therefore, the conduction of Q1 and Q2 are mutually exclusive." Further, at col. 2, line 56 - 59, Nasila states with respect to Fig. 2 that, "[b]ecause Q1 and Q2 are intimately interlocked, Q1 and Q2 cannot conduct simultaneously. Therefore, this interlock supersedes, or obviates the circuitry associated with `DEADBAND GENERATION`, of traditional half-bridges."

Based upon the above passages cited from within the Nasila specification, one of ordinary skill in the art would understand the principle of operation of Nasila is based upon mutually exclusive, interlocking relationship between Q1 and Q2. "Output," in Fig. 2 will never receive current from both Q1 and Q2 simultaneously.

On page 4, the Office Action states,". . . [t]herefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution by removing the second (bottom) transistor together with the Zener diode from the circuit, since as well known in the art, the half-bridge drivers are used only for bipolar driving of the load, and if bipolar driving is not required, as Izawa et. al. demonstrated, only one transistor and no Zener diode is necessary."

Applicants respectfully submit that there can be no motivation to modify the circuit in Nasila in such a manner and to combine the Nasila and Izawa references because modifying Nasila in such a manner renders Nasila unsatisfactory for its intended purpose (i.e., to provide a protection circuit for use in bipolar driving of a load in which "the transistors comprising the half-bridge [protection circuit] are electronically interlocked-precluding cross-conduction

. . ." Therefore, in accordance with MPEP §2143.01, the proposed modification is improper. Specifically, MPEP §2143.01 states:

> The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)
>
> **If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.** *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)
>
> .....
>
> **If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.** *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) (Claims were directed to an oil seal comprising a bore engaging portion with outwardly biased resilient spring fingers inserted in a resilient sealing member.)
> (MPEP §2143.01) (Emphasis Added)

C. <u>Nasila and Izawa Address Unrelated Issues</u>

Third, although both Nasila and Izawa drive loads, Nasila and Izawa address issues that are entirely unrelated. For example, the circuit in Izawa addresses protecting MOSFET 18 from over-heating and over-current conditions. With respect to heat protection, Izawa describes at col. 13, lines 55-62, overheat detection circuit 12 that includes temperature detection diode 124 near MOSFET 18 to detect an overheat state and a comparator 122 to generate an overheat detection signal 12a that is transmitted to an overheat protect device 10. Overheat protect device 10 responds by generating load drive instructions 102a and gate control signal 108a.

With respect to over-current protection, Izawa describes at col. 14, lines 50-56, over-current detection circuit 14 that includes resistor element 145 serially connected between the

drain of MOSFET 18 and the load 32 and a comparator 142 to detect a voltage produced in resistor 145 and that generates an over-current detection signal 14a that is transmitted to overheat protect device 10. Overheat protect device 10 responds by adjusting generating load drive instructions 102a and gate control signal 108a, accordingly.

The circuit in Nasila addresses an entirely different problem. As stated in Nasila at col. 1, lines 52 through col. 2, line 6, the circuit in Nasila is designed to protect against damaging a circuit with a half-bridge topology due to the simultaneous conduction of both (output) transistors in the circuit. (See col. 1, lines 52-55). Nasila addresses this problem with a circuit in which "the transistors comprising the half-bridge are electronically interlocked-precluding cross-conduction; and high-side voltage generation and logic level translation are integral to the interlock mechanism." (See col. 2 lines 1-5). For example, at col. 2, lines 9-17, Nasila states that, "illustrated in FIG. 2 is an Ideal Interlocked Half-Bridge schematic. Q1, and Q2 combine to form a half-bridge phase leg. Diode CR2 provides reverse isolation from the GATE to SOURCE of Q1, while permitting forward current through Q2. Observe that if Q2 is conducting, Q1 will be biased OFF through CR2; and that if Q2 is OFF, Q1 will be permitted to conduct, provided it is biased ON. Therefore, the conduction of Q1 and Q2 are mutually exclusive." This technique is very different from that of Izawa, and addresses a different problem.

Applicants respectfully assert that because of the entirely different objectives taught by Izawa and Nasila, and the entirely different techniques employed by each for achieving those objectives, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Nasila solution to produce a circuit as described in the present application.

D. Nasila/Izawa Combination Based Upon Impermissible Hindsight

Fourth, neither Nasila or Izawa teach protecting a transistor from a negative surge current generated as a result of powering off an inductive load. (See the original specification at page 21, line 14, through page 22, line 4). Therefore, it would have been impossible one of ordinary skill in the art at the time the present invention was made to have conceived of combining the Nasila and Izawa references to produce a circuit that performs the same function performed by the present invention when neither Nasila or Izawa perform that function. Applicants respectfully assert that, for at least the reasons described above, there would have been no motivation to combine the Nasila and Izawa references (as required by MPEP §2143.01). Further, Applicants respectfully assert the any perceived motivation to combine the Nasila/Izawa references is the result of hindsight gained by the Examiner from the present application. According to MPEP §2141.01, the use of such hindsight in assessing the scope of prior art references is not permissible.

* * *

For at least these reasons, Applicants respectfully assert that: 1) even if combined, the Nasila/Izawa combination would not include all features recited in the claims of the present application; 2) the proposed Nasila/Izawa combination is improper because the suggested modifications to Nasila would destroy the intended purpose of the protection circuit described in Nasila, or alternatively, would change the purpose of operation of Nasila; 3) the Nasila and Izawa patents address issues unrelated to the present application; and, 4) the Nasila/Izawa combination is based upon impermissible hindsight. Accordingly, it is respectfully submitted that claim 1 is patentably distinguishable over the Nasila/Izawa combination. Claim 2 depends from independent claim 1 and is likewise patentably distinguishable over the Nasila/Izawa combination for at least its dependence on an allowable base claim, as well as for additional features it recites. Claims 4, 9, and 11 include features similar to those feature

included in claim 1. Accordingly, it is respectfully submitted that claims 4, 9, and 11 are patentably distinguishable over the Nasila/Izawa combination. Accordingly, Applicants respectfully request withdrawal of the rejection.

III. 35 U.S.C. §103(a) Rejection of Claims 10 and 12

The Office Action rejects claims 10 and 12 under 35 U.S.C. §103(a) as unpatentable over Nasila in view of Izawa. However, claims 10 and 12 depend from independent claims 9 and 11, respectively, and are patentably distinguishable over the Nasila/Izawa combination for at least their dependence on an allowable base claim, as well as for additional features they recite. Accordingly, Applicants respectfully request withdrawal of the rejection.

IV. 35 U.S.C. §103(a) Rejection of Claim 3

The Office Action rejects claim 3 under 35 U.S.C. §103(a) as unpatentable over Nasila in view of Izawa and further in view of U.S. Patent 5,828,244 to Palara (Palara). For at least the reasons discussed above, Applicants respectfully assert that the Nasila/Izawa combination is improper. Therefore, the Nasila/Izawa/Palara combination is improper for at least the same reasons. Further, even if the Nasila/Izawa/Palara were proper, Palara does not overcome the above-described deficiencies of Nasila/Izawa. Claim 3 depends from independent claim 1, and therefore, is likewise patentably distinguishable over the Nasila/Izawa/Palara combination for at least its dependence on an allowable base claim, as well as for additional features it recites. Accordingly, Applicants respectfully request withdrawal of the rejection.

V. 35 U.S.C. §103(a) Rejection of Claims 5, 7 and 8

The Office Action rejects claims 5, 7 and 8 under 35 U.S.C. §103(a) as unpatentable over Nasila in view of Izawa and further in view of U.S. Patent 6,392,463 to Kitagawa (Kitagawa). For at least the reasons discussed above, Applicants respectfully assert that the Nasila/Izawa combination is improper. Therefore, the Nasila/Izawa/Kitagawa combination is

improper for at least the same reasons. Further, even if the Nasila/Izawa were proper, Kitagawa does not overcome the above-described deficiencies of Nasila/Izawa. Claim 5 depends from independent claim 4, and therefore, is likewise patentably distinguishable over the Nasila/Izawa/Kitagawa combination for at least its dependence on an allowable base claim, as well as for additional features it recites. Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 7 and 8 include features similar to those feature included in independent claim 1. However, Kitagawa does not overcome the above-described deficiencies of Nasila/Izawa. Accordingly, it is respectfully submitted that claims 7 and 8 are patentably distinguishable over the Nasila/Izawa/Kitagawa combination. Accordingly, Applicants respectfully request withdrawal of the rejection.

VI. 35 U.S.C. §103(a) Rejection of Claim 6

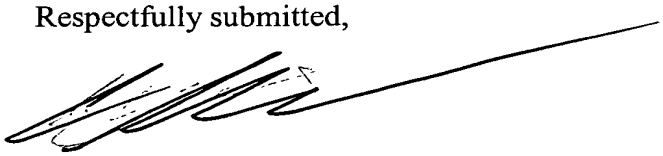
The Office Action rejects claims 6 under 35 U.S.C. §103(a) as unpatentable over Nasila in view of Izawa, further in view of Kitagawa, and still further in view of Palara. For at least the reasons discussed above, Applicants respectfully assert that the Nasila/Izawa combination is improper. Therefore, the Nasila/Izawa/Kitagawa/Palara combination is improper for at least the same reasons. Further, even if the Nasila/Izawa were proper, the Kitagawa and Palara references do not overcome the above-described deficiencies of Nasila/Izawa. Claim 6 depends from independent claim 4, and therefore, is likewise patentably distinguishable over the Nasila/Izawa/Kitagawa/Palara combination for at least its dependence on an allowable base claim, as well as for additional features it recites. Accordingly, Applicants respectfully request withdrawal of the rejection.

VII. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-12 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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